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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/709,167	04/19/2004	Ming-Nen Liang		3166

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EXAMINER	
VO, THANH DUC	
ART UNIT	**PAPER NUMBER**
2189	

DATE MAILED: 04/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/709,167	LIANG ET AL.	
	Examiner	Art Unit	
	Thanh D. Vo	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 April 1904*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5* is/are rejected.

7)☒ Claim(s) *6-8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is responsive to the Application filed on April 19, 2004. Claims 1-8 are presented for examination. Claims 1-8 are pending.

Claim Objections

2. Claims 1-8 are objected to because of the following informalities:

Claims 1-8 contain grammatical errors in numerous places. The Examiner suggests the Applicant re-write the claims as follow:

With respect to the condition of "if yes" or "if no" in claims 1-8, Examiner suggests the Applicant write out the condition to preclude the claim from being unclear or vague. Please see claim 1 below as a reference for re-writing the claim language.

Claim 1. A storage controlling and judging method of a flash memory for writing data to said flash memory, the flash memory comprising a plurality of sets of mother and child blocks, each set of said mother and child blocks having a mother block corresponding to a child block for increasing data storage speed ~~to~~ of said flash memory and using a correlation between said mother and child blocks of said sets of mother and child blocks to substantially reduce erasing frequency of said flash memory for extending a service life thereof; the method comprising:

(a) receiving a writing command;

(b) checking whether an address to be written is in said sets of mother and child blocks;

wherein if the address to be written is not in said sets of mother and child blocks, proceed to step (c);

wherein if the address to be written is in said sets of mother and child blocks, proceed to step (e);

(c) checking whether said flash memory has a set of mother and child blocks;

wherein if said flash memory has a set of mother and child blocks, proceed to step (d);

(d) judging whether numbers of used mother and child blocks reach a preset number in a manager;

wherein if the numbers of used mother and child blocks reach a preset number in said manager:

a set of mother and child block is found and combined to create a new block;

a blank block is found and defined as a child block; and

a block is defined for writing as a mother block, and then said mother block and said child block are combined to create a new set of mother and child blocks, then proceed to step (f);

(e) executing writing;

(f) executing writing from a page in said child block of said sets of mother and child blocks;

(g) executing writing into said page;

(h) judging whether a written page is a last page in said child block, wherein if the written page is the last page in said child block, proceed to step (i); and

(i) judging whether to continue writing into pages, wherein if not to continue writing into pages, proceed to step (j);

(j) end~~ing~~ ~~the~~ writing operation.

As per claims 2, 3, 4, and 7,

A next step number or label should be placed in front of such particular step. For example:

Claim 2. The storage controlling and judging method of the flash memory according to claim 1, wherein the writing operation proceeds to step (l) if said flash memory does not have a set of mother and child blocks in said step (c);

~~wherein~~ (l) a blank block is found and defined as a child block and said mother block and child block are combined as a new set of mother and child block, then proceed to step (f).

Similar deficiencies are in steps (k) of claim 3, (m) of claim 4, (n) of claim 4, and (vii) of claim 7.

As per claim 6, “validstarting” in line 6 should be – valid-starting.

As per claim 6, “validending” in line 10 should be – valid-ending.

As per claim 7, “validpage” in line 3 should be – valid-page.

All dependent claims are objected to as having the same deficiencies as the claims they depend from.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. Claims 1-5 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

As per claim 1, the sequential step from (d) to (e) is not disclosed in the Specification. By comparing the language in claim 1 and the flow chart in Fig. 19, the step of (d) is item 704 and the step of (e) is item 706. There is no indication that there is a linkage between 704 and 706. In addition, the process in item 705 as claimed in step of (d) does not contain a linkage to item 706 (step (e)) as well.

As per claim 3, the Applicant claims "wherein the writing operation proceeds to step (k) if no in said step (d). However, step (d) which corresponds to item 704 of Fig. 19 does not indicate YES or NO, as being claimed, to be proceeded to the next operation.

All dependent claims are rejected as having the same deficiencies as the claims they depend from.

Appropriate correction is required.

Allowable Subject Matter

4. The following claim is drafted by the examiner and considered to distinguish patentably over the art of record in this application, Examiner presented to applicant for consideration:

Claim 6. A storage controlling and judging method of flash memory of a flash memory for writing data into said flash memory, said judging method comprising:

(i)starting the judging method;

(ii) checking whether a starting page R for writing is <u>at</u> or ahead <u>of</u> a <u>valid-starting</u> page N in a child block of a set of mother and child block;

<u>wherein if the starting page R for writing is at or ahead of the valid-starting page N in child block of a set of mother and child block</u>, proceed to step (iii);

(iii) comparing whether an ending page S for writing is <u>at</u> or behind a <u>valid-ending</u> page M in said child block of said set of mother and child block<u>s</u>;

<u>wherein if the ending page S for writing is at or behind a valid-ending page M in said child block of said set of mother and child blocks</u>, proceed to step (iv);

(iv) erasing said child block and replacing a new set of block to create a child block and write data therein;

(v) ending the judging method.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Bennett et al. (US 2005/0144360) discloses a method of increasing the endurance of a non-volatile memory system contains erasable blocks (See Fig. 7A). The memory management system is capable of updating the data in the block as request by the host. During the host write operation, the data is updated in the child block sequentially (page 6, paragraphs 0088-0090).

Gan et al. (2005/0005058) discloses a memory management method with a mother and child block concept to manage the host write and erasure to the flash memory to upgrade the processing speed and shorten the time for transferring the data, and to further extend the life of the flash memory cell.

When the host is to write to page N, the controller will move to block 0 to block N-1 from the mother block to the child block. After finishing, the controller will wait until the host begins to write for the next time and judging whether to continue writing to the same address, if yes, then it is not need for the controller to find a new block but directly writes into the very block. After finishing writing all of the pages of the child block, the controller will erase the mother block, and then replaces the mother block completely by the child block.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh D. Vo whose telephone number is (571) 272-0708. The examiner can normally be reached on M-F 9AM-5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Reginald G. Bragdon can be reached on (571) 272-4204. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thanh Vo
Patent Examiner
AU 2189
4/14/2006

Reginald G. Bragdon
REGINALD G. BRAGDON
PRIMARY EXAMINER